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(57) Abstract :
Advanced video communication requires the high speed as well as low power consumption devices. But the conventional video streaming architectures are failed to maintain this trade¬off. This work presents a novel video streaming architecture using combination of features, which are generated from Feature Accelerated Segment Test (FAST) and Binary Robust Independent Elementary Feature (BRIEF) descriptors. To reduce the complexity of the BRIEF descriptor, we employ an optimized adder tree to perform summation by accumulation on streaming pixels for the smoothing operation. Since the window buffer used in existing designs for computing the BRIEF point-pairs are often poorly utilized, this work proposes an efficient sampling scheme that exploits register reuse to minimize the number of registers. All the designs are implemented and synthesized using Xilinx ISE software with verilog programming language. The simulation results show that the proposed FAST-BRIEF descriptor consumes the low power as compared to the conventional approaches.

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